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## (54) Decision feedback equaliser with reduced-state sequence estimation

(57) A hybrid equalizer for a communications receiver has a decision feedback equalizer having a feedforward filter (10) and a feedback filter (16). The feedforward filter (10) receives an input data stream comprising modulation symbols representing received intelligence which may be subject to distortion, and produces an output data stream partially corrected for such distortion. A reduced state sequence estimator (12) receives the partially corrected output data stream and calculates a sequence of symbols received. A processor (20) executes the Viterbi algorithm for estimating the values of symbols received, based on the partially corrected data stream and on a channel reference, and produces an output. The output of the processor is coupled to the input of the feedback filter (16). The feedback filter coefficients provide the channel reference for the reduced state sequence estimation.

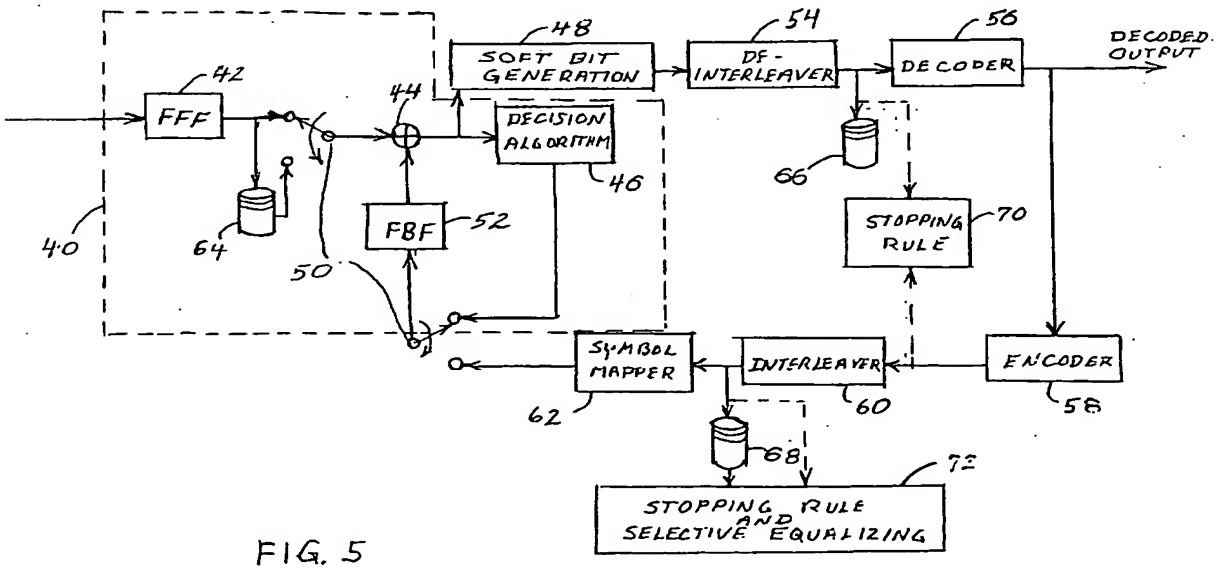


FIG. 5

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## Description

### Field of the Invention

**[0001]** This invention relates to decision-aided equalizers for communication receivers, and more particularly to decision-aided equalizers with reduced error propagation.

### Background of the Invention

**[0002]** In modern communications systems employing Time Division Multiple Access such as, for example, the GSM radiotelephone system, digital information in the form of a bit stream representing voice or data is encoded by the transmitter into a series of complex phase shifted signals and is transmitted by modulating the carrier wave of the transmitter with the encoded symbols. Each symbol transmitted represents a series of bits from the data stream. For instance, eight different such symbols may be used, each symbol representing three bits of the data stream.

**[0003]** The transmitted symbols are received by a receiver and the symbols are reconverted into a bit stream. If the transmission and reception are free from interference and distortion, the symbols are readily converted into a bit stream representing exactly the original bit stream before its conversion into symbols by the transmitter. As a practical matter, however, transmissions are rarely distortion free. Among the distortions which occur is multipath distortion caused when the receiver receives two representations of the same transmitted signal which, because of reflections, arrive at the receiver at slightly different times. The reception of two time-skewed signals causes Intersymbol Interference (ISI), where a symbol's phase component may be distorted by the delayed arrival of an earlier transmitted symbol. Channel fading and noise can also cause difficulty in accurately receiving transmitted signals.

**[0004]** Both of these phenomena can significantly degrade the performance of a high-speed wireless communication system.

**[0005]** Intersymbol interference (ISI) introduced by multipath propagation is mitigated in the receiver of a communication system by means of an Equalizer. Classically, two approaches are considered for this stage: either a symbol-by-symbol decision is performed, based on a filtered received signal, or the whole received sequence is estimated, often using the so-called Viterbi algorithm implementing the Maximum Likelihood Sequence Estimator (MLSE solution).

**[0006]** For symbol-by-symbol decisions, the Decision Feedback Equalizer (DFE) realizes an interesting trade-off between complexity and performance. The best bit error rate (BER) performance is obtained when the DFE filters are optimized for the MMSE (Minimum Mean Square Error) criterion. However, the DFE structure suffers from the error propagation phenomenon: if an error occurs, it enhances the ISI on the following samples entering the decision device, thus causing in turn more errors.

**[0007]** On the other hand, sequence estimation methods give the best performance, but at the cost of increased complexity. For an eight-state symbol constellation, for example, a Viterbi calculation must calculate $8^{L-1}$ possibilities, where L is the number of taps in the channel. Thus suboptimal techniques for the MLSE were proposed:

**[0008]** In " Delayed Decision-Feedback Sequence Estimation" (A. Duel-Hallen, C. Heegard, IEEE Transactions on Communications, vol.37 No. 5, May 1989), the state trellis, basis for the Viterbi algorithm, only takes into account the first *N* taps in the channel. Then, the transition metrics are computed using past tentative decisions on each of the surviving paths. In this respect, it is said that such sequence estimation incorporates a feedback, and the resulting Decision Feedback Sequence Estimation (DFSE) algorithm has a reduced number of states compared to the MLSE.

**[0009]** In "Reduced-State Sequence Estimation with Set Partitioning and Decision Feedback" (M. Vedat Eyuboglu, S.U.H. Quereshi, IEEE Transaction on Communications, vol.36, No.1, Jan.1988), further reduction of the number of states can be achieved by introducing a partitioning of the constellation symbols. This approach is referred to as reduced state sequence estimation (RSSE). There, a "reduced" state is a vector of indexes of symbol subsets. This algorithm provides the greatest flexibility when handling Finite Impulse Response (FIR) channels and high order modulations.

**[0010]** The advantage of reduced state approaches is to reduce the complexity of the Viterbi-based equalizers. On the other hand, their performance can also be degraded by error propagation, even if this phenomenon is less severe than in the DFE, since the reliability of the feedback decisions is improved by the Viterbi stage. This error propagation effect is minimized when the channel to be equalized is minimum-phase. In a mobile communication context, this is usually not the case.

**[0011]** With a reduced state Viterbi processor, typically the input symbol stream is filtered in some manner and applied to the processor so that error propagation is reduced. Other inputs to the Viterbi processor are the estimated channel coefficients, which are usually obtained by calculating the channel parameters from a training frame of a known symbol sequence which is transmitted as a part of a preamble to the data. The calculation determines the weights to be ascribed to each of the coefficients of the preceding symbols so that the weighted effect of the preceding symbols can be subtracted from the combined signal to obtain the value of the symbol being calculated. The Viterbi processor then calculates hard outputs, which are used in the feedback path of the processor in the reduced state version.

**[0012]** Interleaving and channel coding also can be used to mitigate the adverse effects of multipath and fading. A decision-aided equalizer, such as a decision-feedback equalizer (DFE), can be used as a means for mitigating the effects of ISI in a system where an interleaver and channel coder provide further protection against channel fading, residual ISI, and thermal noise.

**[0013]** In general, the decision-aided equalizer uses the linear combination of the past decisions to cancel post-cursor ISI, where the feedback filter (FBF) coefficients are obtained under the assumption that past decisions are correct. Consequently, errors in the past decisions enhance, instead of cancel, the ISI. The enhanced ISI may cause more decision errors in the current and future symbols, which will in turn further enhance the ISI, Thus leading again to propagation errors.

## Summary of the Invention

**[0014]** To address the shortcomings of the prior art, applicants have provided an advantageous new hybrid equalizer and and an improved method for equalizing to mitigate the effects of intersymbol interference, channel fading and noise.

**[0015]** A hybrid equalizer for a communications receiver has a decision feedback equalizer having a feedforward filter and a feedback filter. The feedforward filter receives an input data stream comprising modulation symbols representing received intelligence which may be subject to distortion, and produces an output data stream partially corrected for such distortion. A reduced state sequence estimator receives the partially corrected output data stream and calculates a sequence of symbols received. A processor executes a Viterbi algorithm for estimating the values of symbols received based on the partially corrected data stream and on a channel reference, and produces an output. In the invention the feedback filter is used to provide the channel reference for the processor.

**[0016]** In a method for channel equalization a communications receiver receives an input data stream comprising modulation symbols representing received intelligence that may be subject to distortion, and produces an output data stream partially corrected for such distortion. A first iteration of calculation uses the partially corrected output data stream for estimating a sequence of symbols likely to have been emitted. A processor, which can be a simple decision device or a Viterbi processor, produces both a hard and soft decision on the estimated symbol sequence. A feedback loop is employed to feed back the hard output of the processor that is filtered. The filtered output is summed with the partially corrected data stream to produce a symbol that is mapped into a bit stream. Then the bit stream is deinterleaved and decoded producing a corrected bit stream. The corrected bit stream is selectively reencoded, reinterleaved, and remapped into symbols, the remapped symbols being applied as the feedback in place of the output of the processor. This process is then iterated, the new symbol stream mapped into a bit sequence being fed into the channel decoder again. The number of iterations is controlled by stopping rules.

## Brief Description of the Drawings

**[0017]** FIG. 1 is a block diagram of one aspect of the invention showing a hybrid RSSE DFE equalizer.

**[0018]** FIG. 2 is a representation of the set partitioning for the two-state RSSE DFE of a preferred embodiment of the invention for 8-PSK modulation.

**[0019]** FIG. 3 is a diagram of the state trellis for the two-state RSSE DFE of a preferred embodiment of the invention.

**[0020]** FIG. 4 is a flow chart of the core part of the two-state hybrid RSSE DFE equalizer of the invention.

**[0021]** FIG. 5 is a block diagram of an iterative equalizer, the second aspect of the invention.

**[0022]** FIG. 6 is a flow chart showing the operation of the iterative equalizer of FIG.5.

## Description of the Preferred Embodiment

**[0023]** FIG. 1 shows a hybrid equalization scheme, based on a Minimum Mean Square Error (MMSE) Decision Feedback Equalizer (DFE), in which error propagation is mitigated by the use of a Reduced State Sequence Estimator (RSSE) algorithm as a decision device. The DFE is designed to perform symbol-by-symbol calculations, generally solving an equation of the type:

$$[\, Y_n = h_0 S_n + h_1 S_{n-1} + h_2 S_{n-2} \cdots ]$$

**[0024]** Where $Y_n$ is known, $S_n$ is the symbol currently being calculated, $S_{n-1}$ is the preceding symbol, and $h_0$, $h_1$, $h_2$... are the channel coefficients.

**[0025]** In a generalized representation, the input data stream is filtered by an MMSE DFE Feedforward filter, yielding $Y_k$, which is used to compute the branch metric. In the hybrid RSSE DFE algorithm, the signal constellation is first partitioned into N disjoint subsets. The number of states in the trellis is then $N^L$ where L is the size of the state vector

and N the number of subsets. In a low complexity implementation, a preferred choice is L=1, and in that case, the Viterbi machine is said to be in state s if the last transmitted symbol belongs to subset s . The branch metrics associated with state transitions are computed based on the Euclidean distance between the equalized signal and coset-sliced symbols. One feedback register is maintained for every surviving path.

**[0026]** Mathematically, denote a node in the trellis as (k,s), where k is the time index and s is the state index, and define the following variables:

K: length of the sequence.

N: number of states in the trellis.

$S_s$ , s=0,1(N-1): subsets of the signal constellation, $^{N-1}_{s=0}$ $S_s$ is the signal constellation.

M(k.s), k=0.1(K-1), s=0,1(N-1): accumulated metric of node (k,s);

$G_{js}$ : branch metric associated with the transition from node (k-1,j) to node (k,s);

$d_{js}$ : coset sliced symbols associated with the transition from node (k-1,j) to node (k.s);

p(k,s): state at time (k-1) of the surviving path leading to node (k,s);

$e_s$ (k), k=0,1,...(K-1): equalized signal associated with the surviving path leading to node (k,s).

$SoftOut_s$ (k), k=0,1,...,(K-1): soft-decisions associated with the surviving path leading to node (k,s);

$HardOut_s$ (t), k=0,1,...,(K-1): hard-decisions associated with the surviving path leading

**[0027]** The hybrid RSSE DFE algorithm for L=1 is as follows:

For s=0, 1,..., (N-1), M(-1,s)← 0;

For s=0, 1,..(N-1) and n=1, 2,...$N_b$, $FB_s$ (n) ← 0

For k = 0,1,..., (K-1), repeat:

Compute Equalized Signals: For s=0,1,...*(N-1)*: $e_s$ (k) ← [y(k)-$^{N_b}_{n=1}\Sigma$ $b_n$ $HardOut_s$ (k-n)

Coset Slicing: For s=0,1,...(N-1), j=0,1,...(N-1): $d_{js}$ ← $\min_{XE\ Ss}$ I $e_j$ (k) - x $I^2$. (Note that $d_{js}$ ∈ Ss).

Compute Branch Metric: For s=0,1,...(N-1), j=0,1,...(N-1): $\Gamma_{js}$ ← $Ie_j$ (k) - $d_{js}$ $I^2$

Update Node Metric: For: s = 0.1....(N-1): M (k,s) ←min {M (k-1, *j* + $\Gamma_{js}$}

Update Path History: For: s = 0,1,...(N-1): p (k,s) = arg min {*M ( k*-1, *j* + $\Gamma_{js}$}

Update Hard-decision Outputs : For s = 0,1,...(*N* -1), repeat:

For λ = 0,1,...*k* - 1: $HardOut_s$ (λ)←$HardOut_{p(k.s)}$ (λ):

$HardOut_s$ *(k)* = $d_{p\ (k.s)s}$.

Update Soft-decision Outputs : For s=0,1,...(*N*-1), repeat:

For λ = 0,1,...*t* - 1 : $SoftOut_s$ (λ)←$SoftOut_{p\ (k.s)}$ (λ) ;

$SoftOut_s$ *(k)* = $e_{p\ (k.s)}$ (*k*).

Update Feedback Register: For s = 0,1,... (*N*-1), repeat:

For *n*=1,2,...($N_b$: $FB_s$ ($N_h$- *n)* ←$FB_{p(ks)}$ ($N_b$ - *n*);

$FB_s$ (1) = $d_{p(k.s)s}$.

Final Output:

$$FinalState \leftarrow \arg\min_{s} M\ (K-1, s)\ ;$$

Final hard-decision output is $HardOut_{FinalState}$ *(k)*, *k* = 0,1,...(*K* - 1)

Final soft-decision output is $SoftOut_{FinalState}$ *(k)*, *k* = 0,1, ..., (*K* - 1).

**[0028]** Note that the buffering of the hard-decision outputs HardOut is unnecessary if only the soft-decision outputs are to be used in subsequent processing. Although only the algorithm for L = 1 is shown, it can be easily generated for any value of L.

**[0029]** In a preferred embodiment of FIG. 1, the Feedforward Filter 10 of the DFE is used as a prefilter for the Reduced State Sequence Estimator 12 and the channel seen by the RSSE 12 is the Finite Impulse Response (FIR) of the Feedback Filter 16 of the MMSE DFE. Recall that the channel input is usually obtained by calculating the channel parameters from a training frame of a known symbol sequence which is transmitted as a part of a preamble to the data.

The advantage of using the Feedback Filter 16 as the channel representation is that soft-decision outputs in the form of a bit stream are directly generated as shown below.

**[0030]** The input signal $Y_k$ is applied to summing node 14, which also receives an input from the DFE Feedback Filter 16. The summing node 14 combines these signals and outputs the combined signal g(k) as symbol-level soft outputs 17 without any additional processing. As noted earlier in conventional sequence estimators such as the MLSE, DFSE, or pure RSSE the soft-decision outputs are not automatically derived in this manner, but must be separately calculated, adding to the complexity of those devices. The soft-decision outputs can greatly enhance the performance of the overall equalizer and decoder chain.

**[0031]** The Feedback Filter 16 derives its input from the past history of processed input signals. The past history is provided by storing in storage 18 the decision on the symbol leading to state $S_i$ based on the branch metrics comparison performed by branch metric comparator 19 using as inputs the branch metrics provided by the branch metric calculator 20 which is part of the Viterbi algorithm processor. The filtered input signal $Y_k$ is also applied to the branch metric calculator 20 which receives another input from $d_{js}$ which is a possible value of what the symbol presently being calculated is, and which corresponds to a possible transition in the trellis. This trellis is representationally shown by 22. In the Viterbi algorithm, branch metrics are calculated for each possible predecessor state of each arrival state in the trellis. For a given arrival state $S_0$, the most likely predecessor $j_0$ is chosen, and the symbol $dj_0s_0$, corresponding to the transition, is stored in the path history of state $S_0$, and in the feedback register.

**[0032]** The two-state RSSE of the disclosed embodiment relies on a partitioning on the symbol constellation into two subsets as described in FIG. 2. It is the lowest complexity hybrid scheme and it is a preferred embodiment of the invention. The two-state hybrid RSSE DFE was chosen because of its flexibility, superior performance, and low complexity. In this device the number of states in the trellis (2) is considerably less than the constellation size (8). As noted earlier this would not be possible for devices such as the Decision Feedback Sequence Estimator (DFSE) or the Maximum likelihood Sequence Estimator (MLSE).

**[0033]** In this implementation, the symbols of the constellation are partitioned into two subsets with four 8-PSK (Phase Shift Keyed) symbols each, so that the distance between symbols belonging to the same subset is maximized. The set partitioning is shown in FIG. 2 with one set being represented by black circles and the other set by shaded circles.

**[0034]** FIG. 3 is a diagram of the state trellis for the two-state RSSE DFE of a preferred embodiment of the invention, the function of which is described above. The state trellis of FIG. 3 shows the source and destination nodes of each of the possible signal paths in a two-state trellis.

**[0035]** Coset slicing in this implementation is done by first determining the closest 8-PSK symbol, d, to the equalized signal $e_s$ (t). Then the algebraic sign of the quantity:

**[0036]** Coset slicing in this implementation is done by first determining the closest 8-PSK symbol, d, to the equalized signal $e_s$ (t). Then the algebraic sign of the quantity:

$$\text{Phase Diff} = \text{Im}\,[d \times \text{SoftOut}_s^{\times}(t)]$$

Is computed. A look-up table, shown in Table 1, is then used to determine the coset sliced symbols $d_{s0}$ and $d_{s1}$.

| 8-PSK symbol | 0 0 0 | 0 0 1 | 0 1 0 | 0 1 1 | 1 0 0 | 1 0 1 | 1 1 0 | 1 1 1 |
|---|---|---|---|---|---|---|---|---|
| Subset | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| Nearest Symbol (Phase diff>0) | 2 | 0 | 3 | 7 | 5 | 1 | 4 | 6 |
| Nearest Symbol (Phase diff<0) | 1 | 5 | 0 | 2 | 6 | 4 | 7 | 3 |

**[0037]** FIG. 4 is a flow chart of the core part of the two-state hybrid RSSE DFE equalizer of the invention. This represents the specific case of the generalized algorithm presented above.

**[0038]** The improvement obtained results from the close integration of DFE and RSSE: improvement of the DFE by introducing an RSSE "decision device", but in turn improvement of the RSSE by using the DFE filters as prefilter and equivalent channel. An advantage of using RSSE is to have the flexibility to design very low cost receivers, in which the number of states in the Viterbi algorithm is smaller than the signal constellation size.

**[0039]** As a further improvement, there is shown a new method and apparatus for mitigating the effect of error propagation in decision-aided equalizers such as the DFE. In this method, equalization is performed iteratively, and hard information is fed back from the channel decoder to the equalizer to reduce error propagation. The iterative approach of the invention applies to any decision-aided equalizer for reducing the error propagation effect in a receiver. In this

approach, the processing is done on a block-by-block basis, one iteration estimating a whole block of emitted symbols.

**[0040]** FIG. 5 shows a block diagram of the iterative equalizer. A received signal, which may be interleaved and convolutionally coded, is applied to the Feed Forward Filter 42 of a Decision Feedback Equalizer decision device 40. The output of the Feed Forward Filter 42 is applied to a summing node 44, the output of which is applied to a processor 46, which may be a Viterbi processor or any other kind of processor for sequence estimation, and to a Soft Bit Generator 48. The output of the processor is applied through a switch 50 to the Feedback Filter 52 of the decision aided equalizer. The output symbols of the Feedback Filter 52 are one of the inputs to the summing node 44. The hybrid equalizer of FIG.1 is a possible embodiment for this stage, but other solutions exist, such as a plain DFE. The output bits of the Soft Bit Generator 48 are deinterleaved by Deinterleaver 54, the output of which is decoded by Channel Decoder 56, which may be a convolutional decoder, to provide a decoded output signal representing the received sequence corrected for errors as a result of noise or residual Intersymbol Interference (ISI).

**[0041]** Thus, in the first iterative cycle, the decision aided equalizer 40 functions in a conventional way in estimating the entire sequence. In every subsequent iteration, however, switch 50 is moved to its alternate position to disconnect the Feedback Filter 52 from the processor 46, and to remove the incoming data stream from the summing node 44 and a new signal is applied to the Feedback Filter 52.

**[0042]** The new signal is produced by taking the decoded output signal, re-encoding the signal in Encoder 58, the output of which is applied to Interleaver 60 to be reinterleaved and then coupled through Symbol Mapper 62 and Switch 50 to Feedback Filter 52. Symbol Mapper 62 is used to return the bit stream to a symbol stream to be compared to the originally received symbol stream from buffer 64.

**[0043]** This technique relies on the fact that the reencoded sequence contains fewer errors because of the decoder's error correcting ability. The errors corrected in the decoder are not reintroduced into the Feedback Filter 52, thus reducing the effect of error propagation.

**[0044]** Mechanisms for convergence control and selective re-equalization are also implemented, as will be discussed later. It should be noted that buffers are necessary to store the outputs of the Feedforward Filter 42, the soft inputs to the Channel Decoder 56, and the outputs of the interleaver 60. These are stored respectively in Buffers 64, 66, and 68. A Buffer (not shown) may also be necessary to store the coefficients of the Feedback Filter 52 if the coded symbols are interleaved over bursts with different channel characteristics. The output of Feedforward Filter 42 is saved in buffer 64 to provide a copy of the original data stream for use in subsequent iterations of the equalizer.

**[0045]** Following the deinterleaving of the Soft Bits by the Deinterleaver 54, and following the re-encoding of the decoded output by Encoder 58, a test is made for convergence to determine whether the iterative process should stop or continue, thus eliminating unnecessary iterations. The first test is made by Stopping Rule 70, which is:

**[0046]** At iteration $i$, if the output of the channel re-encoder differs from the hard input (the sign bit of the soft input) of the Channel Decoder 56 by less than $\theta_{low}$ or more than $\theta_{high}$ bits, the iteration is stopped. Otherwise perform interleaving and check Rule 72. Theta is determined experimentally, and in general, different values are necessary for different codes and different maximum numbers of iterations.

Stopping rule 72 is:

**[0047]** Stop the iteration if no re-equalization is necessary. Re-equalization of a burst is necessary if and only if the interleaver output at iteration $i$ is different from that of iteration $i - 1$.

**[0048]** Stopping Rule 70 uses the number of different bits between the re-encoded sequence and the de-interleaved hard decision received sequence as a measure of channel quality. If there are many different bits, then the channel is probably very poor, and further iterations are useless. If there are only a few different bits, then the channel is probably very good, and further iterations are unnecessary.

**[0049]** Stopping Rule 72 monitors the change in the re-encoded sequence from one iteration to the next. If there is no change, no further iteration is necessary because further error correction is impossible.

**[0050]** A further reduction in complexity and processing time is achieved by selective re-equalization of the received signal. In conjunction with the test of Stopping Rule 72, a new iteration will begin if the Interleaver 60 output at iteration $i$ is different from that of iteration $i-1$. If there is a difference, the location of the differences is noted and only the bits or symbols associated with the affected location (plus any adjacent locations that may be affected, depending on the length of the Feedback Filter 52).

**[0051]** FIG. 6 is a flow chart showing the operation of this embodiment of the invention as set out above, and it clarifies the operation of Stop Rules 70 and 72. This flow chart represents the operation of the device as described above and is self-explanatory when viewed with the above description.

## Claims

1. A hybrid equalizer for a communications receiver comprising:

   a decision feedback equalizer having a feedforward filter and a feedback filter;

   the feedforward filter receiving an input data stream comprising modulation symbols representing received intelligence which may be subject to distortion, and for producing an output data stream partially corrected for said distortion;

   a reduced-state sequence estimator for estimating the values of the symbols received based on the partially corrected data stream and on a channel reference, and for producing hard and soft output sequences of emitted symbols;

   the hard output of the processor being coupled to the input of the feedback filter;

   the feedback filter coefficients providing the channel reference for the processor.

2. An equalizer as set forth in claim 1 in which the output of the feedback filter summed with the input data stream produces a symbol stream representing the received symbols being processed by the reduced-state sequence estimator.

3. An equalizer as set forth in claim 1 in which the processing for the reduced-state sequence estimation is based on a Viterbi algorithm.

4. An equalizer as set forth in claim 2 further comprising a decoder for decoding and error-correcting the soft output bit stream.

5. An equalizer as set forth in claim 4 further comprising an encoder for selectively reencoding the corrected bit stream and a symbol mapper for remapping the bit stream into symbols, and for applying the remapped symbols as the input to the feedback filter in place of the output of the processor.

6. A method for channel equalization in a communications receiver comprising:

   receiving an input data stream comprising modulation symbols representing received intelligence which may be subject to distortion, and for producing an output data stream partially corrected for said distortion;

   in a first iteration of calculation estimating the values of the symbols received based on the partially corrected data stream and on a channel reference, and producing hard and soft output sequences of emitted symbols;

   employing a filtered feedback loop to feed back the hard output of the processor;

   the feedback filter coefficients providing the channel reference for the processor.

7. A method as set forth in claim 6 further comprising summing the filtered output with the partially corrected data stream to produce a bit stream representing the received symbols.

8. A method as set forth in claim 6 wherein the calculation is a Viterbi algorithm.

9. A method as set forth in claim 7 further comprising decoding and error-correcting the soft output bit stream.

10. A method as set forth in claim 9 further comprising selectively reencoding and reinterleaving the corrected bit stream and remapping the bit stream into symbols, and for applying the remapped symbols as the feedback in place of the output of the processor.

11. A method as set forth in claim 10 further comprising in subsequent iterations of calculation deinterleaving and decoding the bit stream producing a corrected bit stream.



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12. An iterative decision-aided equalizer comprising:

an equalizer having a decision device for receiving iteratively an input data stream and for producing hard outputs, and having a feedback loop with a feedback filter, the hard outputs of the equalizer being coupled to the input of the feedback filter;

the output of the feedback filter being summed with the input data stream to produce a symbol stream representing the received symbols for processing by the decision device of the equalizer;

a device generating a stream of soft bit values from a soft decision on symbols provided by the decision device;

a channel decoder for decoding and error-correcting the bit stream and a symbol mapper for remapping the bit stream into symbols, and for applying the remapped symbols as the input to the feedback filter in place of the output of the processor.

13. An equalizer as set forth in claim 12 further comprising means for controlling the number of iterations of the decision-aided equalizer.

14. A method for improving the performance of an iterative decision-aided equalizer comprising:

applying iteratively an input data stream to a decision device to produce hard outputs;

applying the hard outputs of the decision device through a feedback loop;

the feedback loop being summed with the input data stream to produce a symbol stream representing the received symbols for processing by the decision device of the equalizer;

generating a stream of soft bit values from a soft decision on symbols provided by the decision device;

decoding and error-correcting the bit stream and remapping the bit stream into symbols, and

applying the remapped symbols as the input to the feedback loop in place of the output of the processor.

15. A method as set forth in claim 14 further comprising controlling the number of iterations of the decision-aided equalizer.

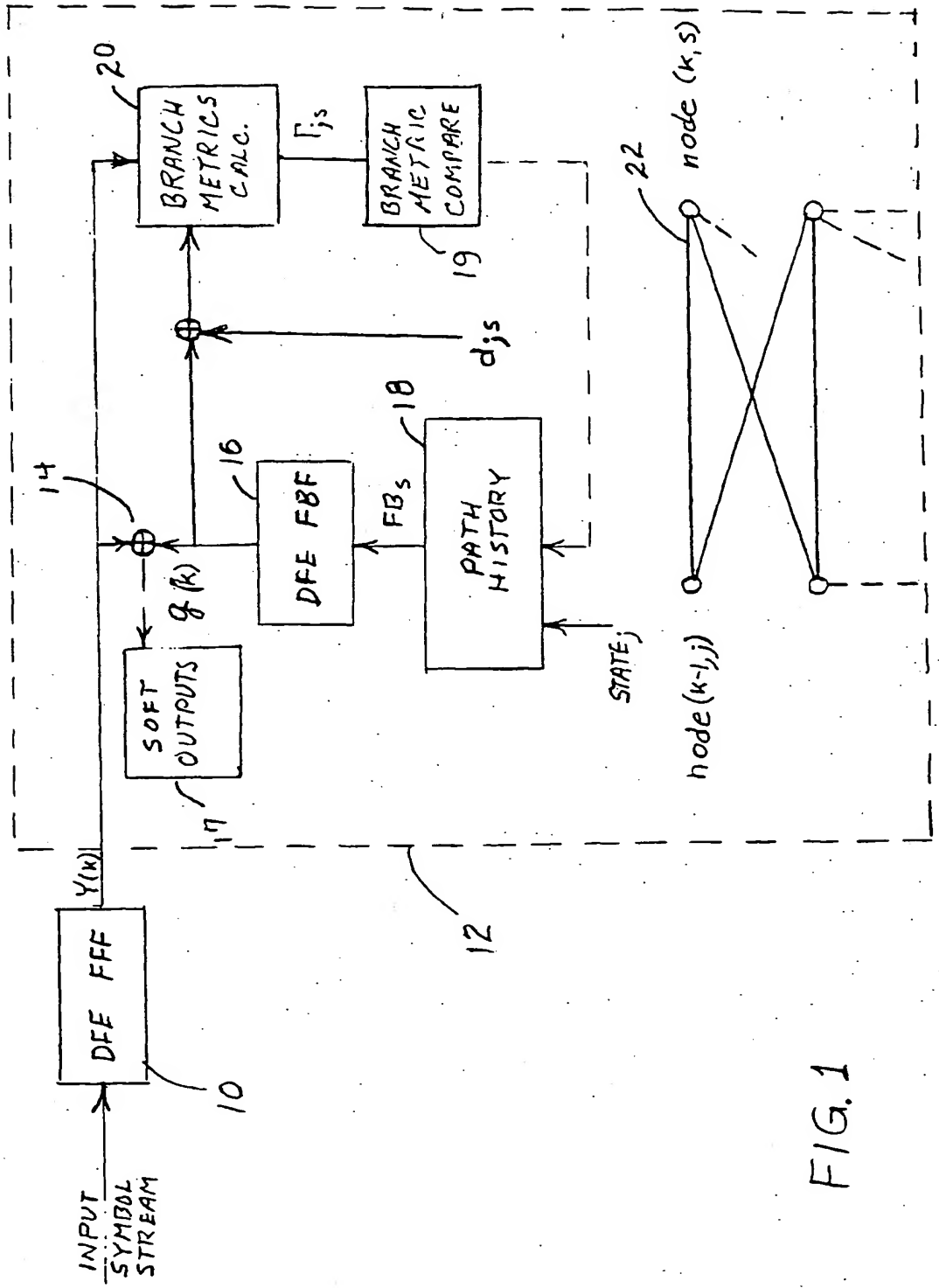


FIG. 1

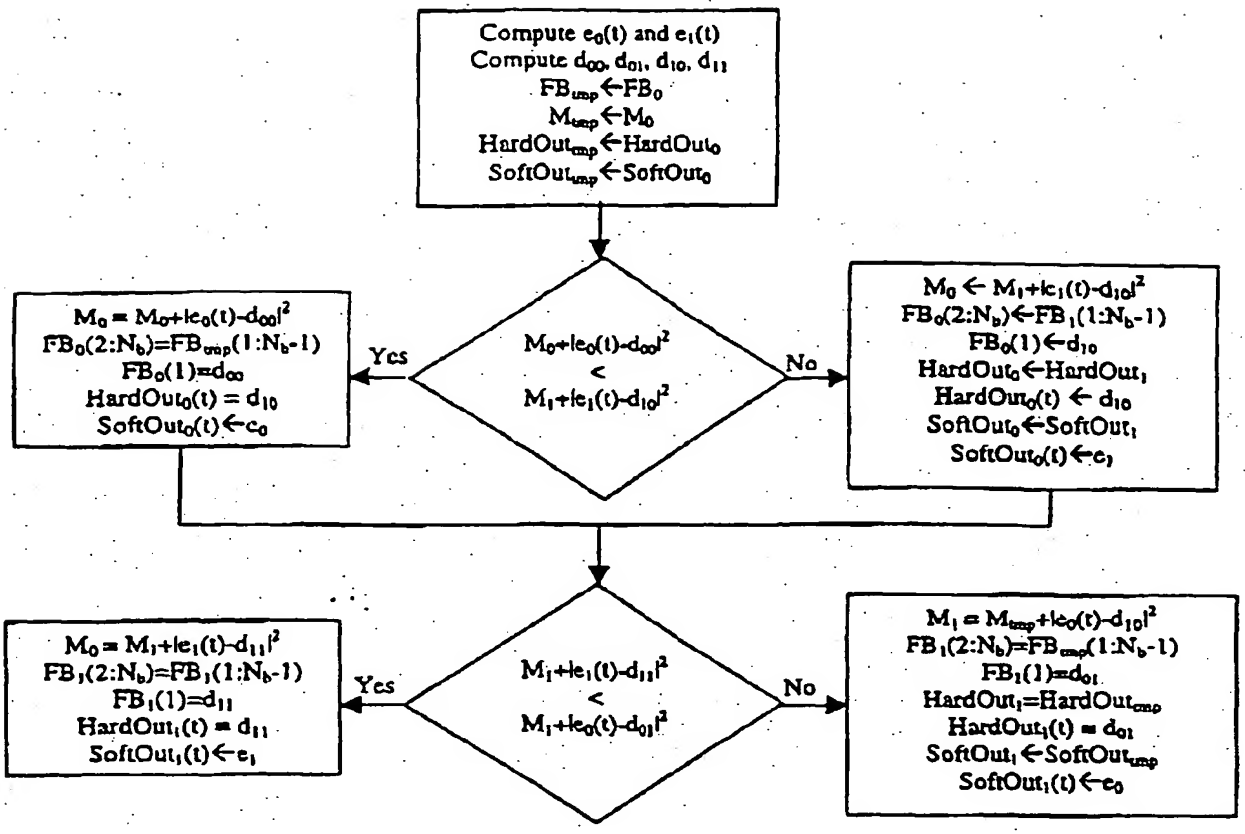


FIG. 4

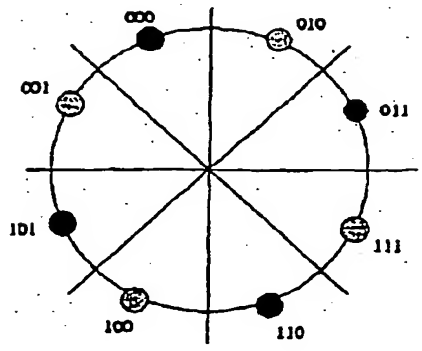


FIG. 2

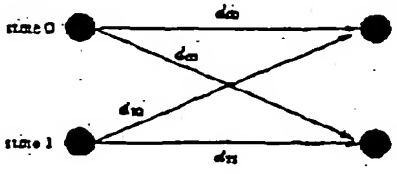


FIG. 3

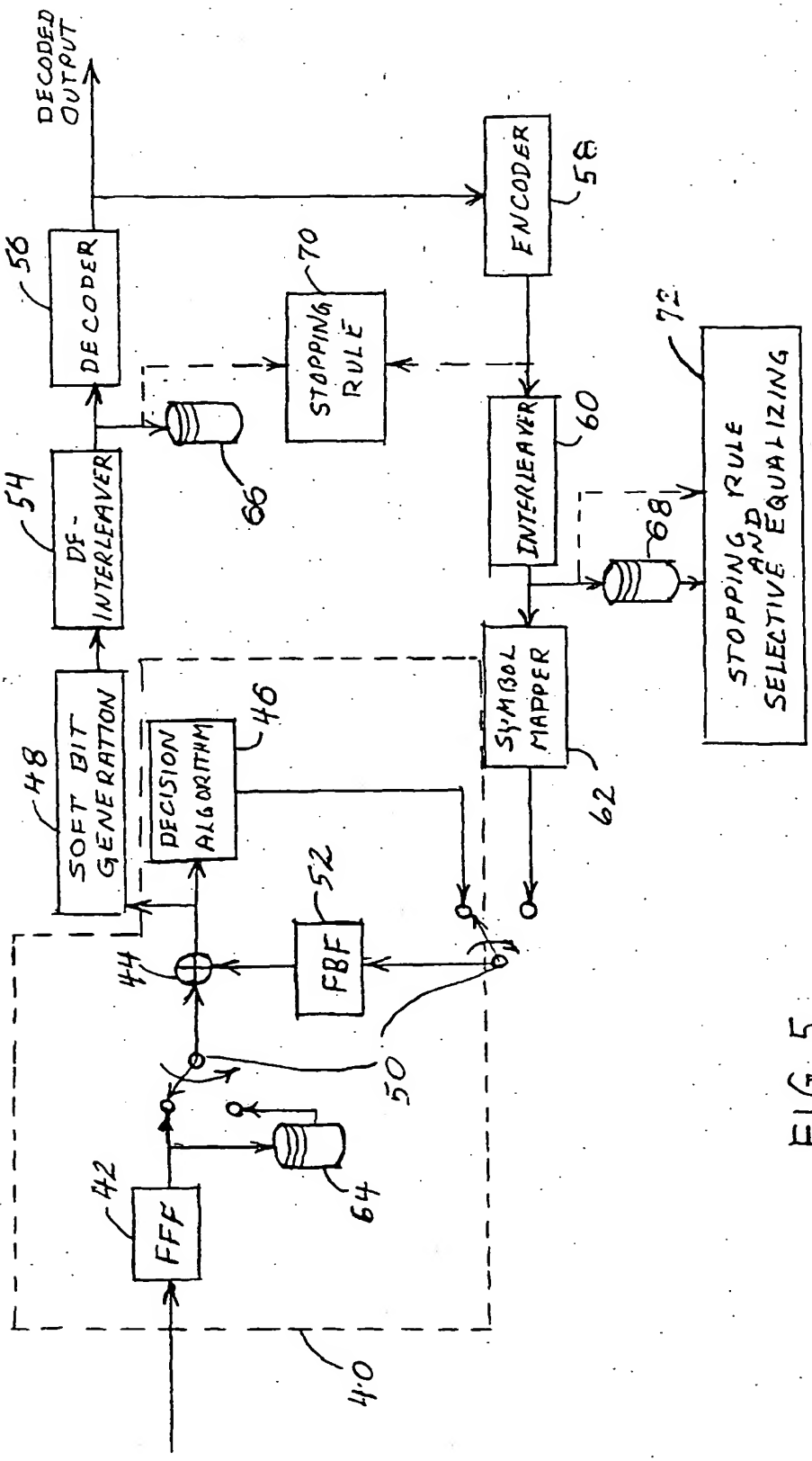


FIG. 5

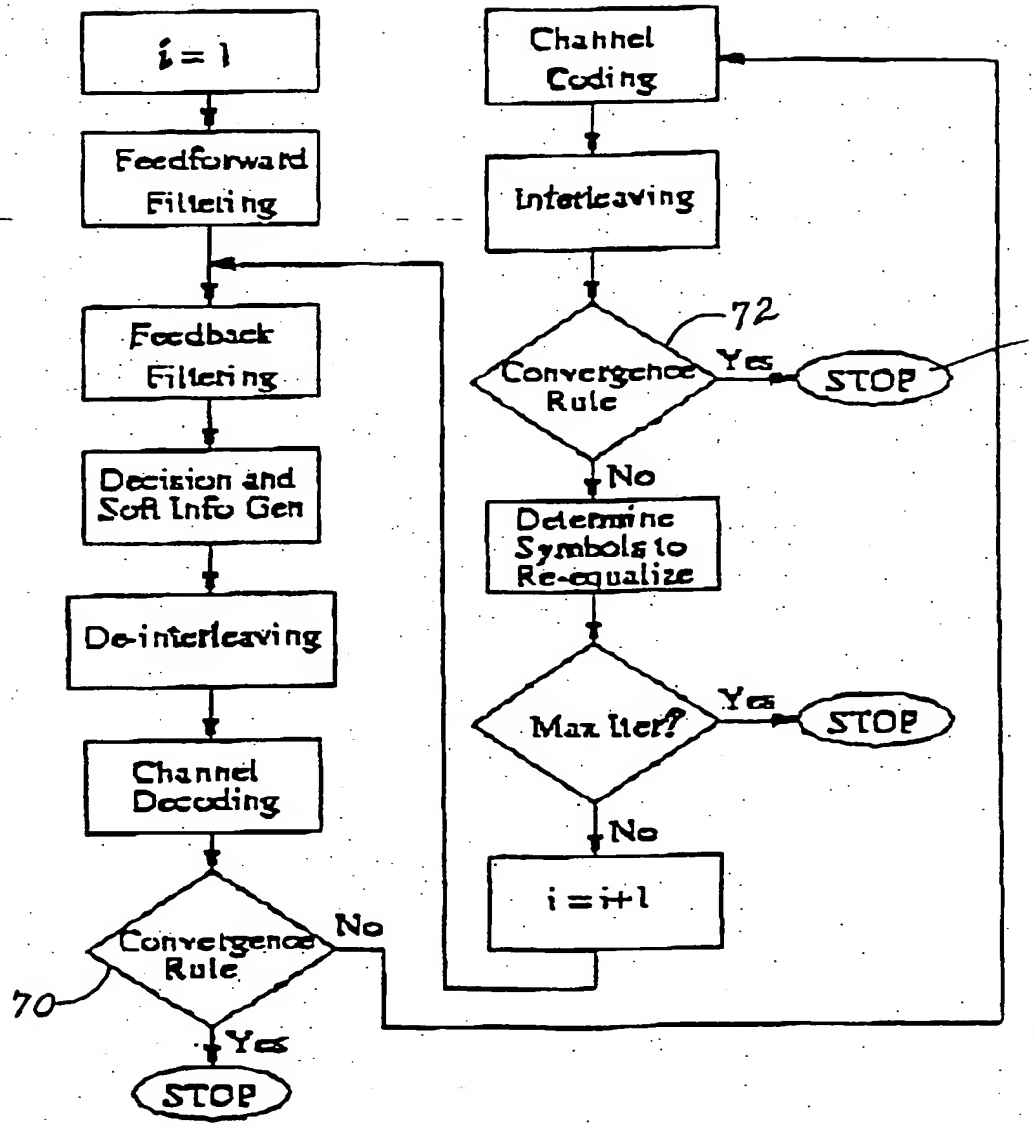


FIG. 6

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# EUROPEAN SEARCH REPORT

Application Number
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The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
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| THE HAGUE | 2 June 2000 | Koukourlis, S |

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Application Number
EP 99 40 1654

## CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claim(s):

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

## LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

☒ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

☐ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

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Application Number
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The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
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| THE HAGUE | 2 June 2000 | Koukourlis, S |

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## LACK OF UNITY OF INVENTION
## SHEET B

Application Number
EP 99 40 1654

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims: 1-11

   Hybrid equaliser comprising sequence estimator and decision feedback equaliser of which the feedback filter coefficients provide the channel reference.

2. Claims: 12-15

   Iterative decision-aided equaliser.

European Patent Office

# EUROPEAN SEARCH REPORT

Application Number
EP 99 40 1654

## DOCUMENTS CONSIDERED TO BE RELEVANT

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The present search report has been drawn up for all claims

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Application Number
EP 99 40 1654

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